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EXAMINER	
CHOWDHURY, AFROZA Y	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/528,255	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	AFROZA Y. CHOWDHURY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on **November 25, 2008** has been entered. Currently, claims 1-35 are pending. Applicant's newly added claims and arguments are addressed herein below.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**each pixel consists of two ratioed sub pixels** " (claim 21) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 1, "**wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals**" is not described in such a way that enables one skill in the art to understand how two different modes of display be in one display device. In those two different modes of display, the TFT's are connected in two different ways. How those two different circuit arrangements fit in one display device?

5. Claims 1-18, 21, 22-26, 28, 29-32, and 33-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, "**wherein device is selectively operable in a first mode … and in a second mode…**" is not described in the specification as submitted originally. The originally filed specification does not describe "**selectively switching**".

Regarding claim 13, "**the timing and control unit selectively switching between the first mode of operation and the second mode of operation in response to a mode selection control signal**" is not described in the specification as submitted originally. The originally filed specification does not describe "**selectively switching between the first mode of operation and the second mode of operation".**

Regarding claim 15, "**the switching transistor or transistors of a pixel other than the common switching transistor are turned on during the first mode of operation for a period of time longer than that during the second mode of operation**" is not described in the specification as submitted originally.

Regarding claim 17, "**the sub pixels of a pixel are addressed individually with respective data signals each having a level selectable from a second number of levels, the second number being smaller than the first number**" is not described in the specification as filed originally.

Regarding claim 18, "**the second number is equal to 2**" is not described in the specification as submitted originally.

Regarding claim 21, "**each pixel consists of two ratioed sub pixels** "is not described in the specification as filed originally.

Regarding claim 22, "**a first switching transistor with its input terminal connected to the column conductor, its output connected to the first sub pixel in the pair, and its control terminal connected to the first row conductor; and a second switching transistor associated with its input terminal connected to the output terminal of the first switching transistor, its output terminal connected to the second sub pixel in the pair, and its control terminal connected to the second row conductor**" is not described in the specification as submitted originally. The originally filed specification does not describe "**first switching transistor**" and "**second switching transistor**".

Regarding claim 25, "**the ratios of the areas of the sub pixels in a pixel are powers of two**" is not described in the specification as submitted originally.

Regarding claim 28, "**selectively switching between the first mode and the second mode in response to a mode selection control signal**" is not described in the specification as filed originally.

Regarding claim 29, "**driving the voltage on all row conductors connected to gate terminals of switching transistors associated with each sub pixel of a target pixel to a voltage level representing the logical on state; driving the voltage on a column conductor connected to the target pixel to a level representing a data signal; and after the sub pixels of the target pixel have been charged to a voltage corresponding to the voltage on the column conductor, driving the voltage on the row conductor connected to the gate terminal of a select transistor of the target pixel to a voltage level representing the logical off state, wherein the select transistor is the only transistor in the pixel circuit that is directly connected to the column conductor**" is not described in the specification as submitted originally. The originally filed specification does not describe "**target pixel**", "**logical on state**", and "**logical off state**".

Regarding claim 31, "**the data signal represents a grayscale value of one color component of a pixel in an image**" is not described in the specification as

submitted originally. The originally filed specification does not describe "**a grayscale value of one color component of a pixel**".

Regarding claim 32, "**driving the display device in the first mode comprises maintaining the voltage on the row conductor connected to the gate terminal or terminals of switching transistors other than the select transistor of the target pixel at a level representing the logical on state after the voltage on the row conductor connected to the gate terminal of the select transistor of the target pixel is driven to a level representing the logical off state**" is not described in the specification as submitted originally. The originally filed specification does not describe "**target pixel**", "**logical on state**", and "**logical off state**".

Regarding claim 33, "**driving the voltage on a row conductor connected to a gate terminal of a select transistor of a target pixel to a voltage level representing a logical on state, wherein the select transistor is the only transistor in the target pixel that is directly connected to the column conductor; and for each sub pixel in the target pixel: driving the voltage on row conductors connected to switching transistors, if any, that are located between the column conductor and the sub pixel to a voltage level that represents the logical on state; driving the voltage on a column conductor connected to the target pixel to a voltage level representing a logical light state or dark state for the sub pixel; and after the sub pixel has been charged to a voltage corresponding to the voltage on the column conductor,**

driving the voltage on the row conductor connected to the switching transistor associated with the sub pixel to a voltage level representing the logical off state" is not described in the specification as submitted originally. The originally filed specification does not describe "**target pixel**", "**logical on state**", "**logical off state**", "**logical light state**", and "**logical dark state**".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-7, 9-12, 14, 19, 20, 22, 23, 26, 27, 29, 30, 32, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by **Edwards et al.** (US 7,230,597).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to claim 1, Edwards et al. discloses an active matrix display device comprising

an array of pixels a set of row conductors through which rows of pixels are selected (fig. 1, col. 4, lines 64-67),

a set of column conductors through which data signals are supplied to selected pixels (fig. 1, col. 4, line 64 – col. 5, line 13),

each pixel comprising a plurality of sub pixels which sub pixels are each associated with a respective switching transistor for controlling the supply of a data signal to the sub pixel (figs. 1, 8, 9, col. 4, line 64 – col. 5, line 13),

wherein the plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor through which data signals are supplied to the sub pixels (fig. 1), and

wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal (fig. 9, col. 8, lines 44-48) and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals (fig. 8, col. 8, lines 35-40) (as best understood).

As to claim 2, Edwards et al. teaches a display device wherein the device comprises drive means for providing data signals to the column conductors and switching signals to the row conductors (fig. 1), and

wherein the drive means is operable in the first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a

data signal on the associated column conductor to each sub pixel (fig. 9, col. 8, lines 44-48), and

wherein the drive means is operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels (fig. 8, col. 8, lines 35-40).

As to claim 3, Edwards et al. teaches a display device wherein the sub pixels of a pixel are connected in serial manner with the input terminal of the switching transistor associated with the first sub pixel of the series being connected to the associated column address conductor and with the input terminal of the switching transistor associated with each of the other sub pixels in the series being connected to the output terminal of the switching transistor associated with the preceding sub pixel in the series (fig. 9).

As to claim 4, Edwards et al. teaches a display device where the sub pixels of a pixel are connected in parallel manner with the input terminal of the switching transistor associated with one sub pixel being connected to the associated column address conductor and with the input terminals of the switching transistors associated with the other sub pixels being connected to the output terminal of the switching transistor associated with the one pixel (fig. 8).

As to claim 5, Edwards et al. teaches a display device wherein the control electrodes of the switching transistors associated with the sub pixels of a pixel are connected to respective different row conductors (fig. 8).

As to claim 6, Edwards et al. teaches a display device where each pixel comprises first and second sub pixels, wherein the control electrodes of the switching transistors associated with the first and second sub pixels of a pixel are connected to first and second row conductors respectively (figs. 1, 8, 9),

wherein, for each pixel, the input of the switching transistor associated with the first sub pixel is connected to the associated column conductor and the input of the switching transistor associated with the second sub pixel is connected to the output of the switching transistor associated with the first sub pixel (figs. 1, 8, 9),

wherein the first row conductor connected to one pixel is connected also to the control electrode of the switching transistor associated with the second sub pixel of another pixel connected to the associated column conductor (figs. 8, 9), and

wherein the second row conductor connected to the one pixel is connected also to the control electrode of the switching transistor associated with the first sub pixel of a further pixel connected to the associated column address conductor (figs. 8, 9).

As to claim 7, Edwards et al. teaches a display device where the sub pixels comprise liquid crystal picture elements connected to the outputs of their associated

switching transistor (fig. 9).

As to claim 9, Edwards et al. teaches a display device wherein the common switching transistor corresponds to the respective switching transistor of one of the plurality of sub pixels (figs. 8, 9).

As to claim 10, Edwards et al. discloses a display device where each of the common switching transistor and the respective switching transistors comprise an input terminal, an output terminal and a gate terminal (figs. 8, 9),

wherein the gate terminal of the common switching transistor is connected to the column conductor associated with the pixel (figs. 8, 9) and

the output terminal of the common switching transistor is connected to at least one of the input terminals of the respective switching transistors (figs. 8, 9).

As to claim 11, Edwards et al. teaches a display device wherein the output terminal of the common switching transistor is connected to each of the input terminals of the respective switching transistors (fig. 8).

As to claim 12, Edwards et al. teaches a display device wherein the output terminal of a first one of the respective switching transistors is connected to the input terminal of a second one of the respective switching transistors (fig. 9).

As to claim 14, Edwards et al. discloses a display device comprising a timing and control unit, a row drive circuit, and a column drive circuit that are operable in the first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a data signal on the associated column conductor to each sub pixel (fig. 9), and

wherein the timing and control unit, row drive circuit, and column drive circuit are operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels (fig. 8).

As to claim 19, Edwards et al. teaches an active matrix device comprising:

a plurality of pixels, each pixel having at least two sub pixels (figs. 1, 8, 9);

a plurality of column conductors and a plurality of row conductors for addressing the pixels (figs. 1, 8, 9, col. 4, line 64 – col. 5, line 13);

a first row conductor that controls a signal path between one of the pixels and one of the column conductors, the first row conductor controlling a signal path between two sub pixels of another pixel (figs. 8, 9); and

a second row conductor that controls a signal path between the other pixel and one of the column conductors (figs. 8, 9).

As to claim 20, Edwards et al. teaches an active matrix device wherein the sub pixels of each pixel are ratioed (figs. 8, 9)

As to claim 22, Edwards et al. discloses an apparatus comprising:

an array ofpixels in which each pixel comprises at least one pair of sub pixels (figs. 1, 8, 9);

column conductors each being connected to the pixels of one column of the array of pixels (figs. 1, 8, 9); and

row conductors in which two or more of the row conductors are connected to the pixels of one row of the array of pixels (figs. 1, 8, 9);

wherein each of the pairs of sub pixels is associated with a circuit for connecting to a column conductor and two row conductors (figs. 1, 8, 9), the circuit comprising:

a first switching transistor with its input terminal connected to the column conductor, its output connected to the first sub pixel in the pair, and its control terminal connected to the first row conductor (fig. 9); and

a second switching transistor associated with its input terminal connected to the output terminal of the first switching transistor, its output terminal connected to the second sub pixel in the pair, and its control terminal connected to the second row conductor.(fig. 9) (as best understood).

Claim 23 is rejected the same as claim 1 above (as best understood).

As to claim 26, Edwards et al. teaches an apparatus wherein at least some row conductors are connected to two pixels in the same column (fig. 8).

Claim 27 is rejected the same as claim 1 above except:

Edwards et al. teaches a method comprising: driving a display device in a first mode in which a plurality of sub-pixels of each of an array of pixels of the display device are addressed simultaneously with a data signal (figs. 1, 8, 9).

Claim 29 is rejected the same as claim 1 above (as best understood).

As to claim 30, Edwards et al. teaches a method wherein the data signal represents a grayscale value of a pixel in an image (col. 7, lines 58-65).

Claims 32 and 33 are also rejected the same as claim 1 above (as best understood).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 13, 15-18, 21, 28, 31, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Edwards et al.** (US 7,230,597).

As to claim 13, Edwards et al. teaches a display device wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal (fig. 9, col. 8, lines 44-48) and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals (fig. 8, col. 8, lines 35-40).

Edwards et al. does not explicitly teach selectively switching between the first mode of operation and the second mode of operation in response to a mode selection control signal.

However, it is obvious that the display device of Edwards et al. is capable of selectively switching between the first mode of operation and the second mode of operation in response to a mode selection control signal in order to reduce power consumption (as best understood).

As to claim 15, it is obvious to design a display device in which each sub pixel corresponds to a switching transistor and the switching transistor or transistors of a pixel other than the common switching transistor are turned on during the first mode of operation for a period of time longer than that during the second mode of operation (as best understood).

As to claim 16, it is obvious to design a display device comprising at least one digital-to- analog converter that provides a data signal to the plurality of sub-pixels of the

pixel when the display device is operating in the first mode, and the at least one digital-to-analog converter is turned off when the display device is operating in the second mode.

As to claim 17, it is obvious to design a display device in which when the display device is operating in the first mode, the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal having a level selectable from a first number of levels, and when the display device is operating in the second mode, the sub pixels of a pixel are addressed individually with respective data signals each having a level selectable from a second number of levels, the second number being smaller than the first number (as best understood).

As to claim 18, it is an obvious choice of design to make a display device in which the second number is equal to 2 (as best understood).

As to claim 21, it is a design choice to make an active matrix device wherein each pixel consists of two ratioed sub pixels (as best understood).

Claim 28 is rejected the same as claim 13 above (as best understood).

As to claim 31, it is obvious choice of design to develop a method wherein the data signal represents a grayscale value of one color component of a pixel in an image (as best understood).

As to claim 34, it is obvious to design a method wherein the switching transistors of the target pixel are arranged in series, and wherein driving the display device in the second mode comprises initially driving the voltage on all row conductors connected to the target pixel to the logical on state and then driving the voltages on the row conductors to the logical off state one row conductor at a time as the sub pixels are charged in order from farthest from the column conductor to closest to the column conductor.

As to claim 35, it is a design choice to develop a method wherein the select transistor is the switching transistor associated with one of the sub pixels and that sub pixel is charged last.

10. Claims 8, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Edwards et al.** (US 7,230,597) in view of **Ozawa et al**. (US 2002/0018056).

As to claim 8, Edwards et al. teaches an active matrix display device comprising an array of pixels a set of row conductors through which rows of pixels are selected, a set of column conductors through which data signals are supplied to selected pixels,

and each pixel comprising a plurality of sub pixels which sub pixels are each associated with a respective switching transistor for controlling the supply of a data signal to the sub pixel (figs. 1, 8, 9, col. 4, line 64 – col. 5, line 13).

Edwards et al. does not specifically teach a display device wherein at least two sub pixels of a pixel are of different areas.

Ozawa et al. discloses an display device where sub-pixels are formed with different areas (fig. 3, [0066]).

Therefore, it would have been obvious to one skill in the art at the time the invention was made to use the idea of Ozawa et al. of using sub-pixels of different areas in each pixel to modify the active matrix display device of Edward et al. in order to provide high quality display.

Claim 24 is rejected the same as claim 8 above.

As to claim 25, it is obvious choice of design to make an apparatus wherein the ratios of the areas of the sub pixels in a pixel are powers of two (as best understood).

Response to Arguments

11. Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA Y. CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
2/28/2009

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